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APPLICATION NO.	FILING	DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/897,953	08/897,953 07/24/1997		HIDEHIKO KIRA	950107A	5157
23850	7590	01/13/2006		EXAMINER	
	•	Z, QUINTOS, I	GRAYBILL, DAVID E		
1725 K STR SUITE 1000	•		ART UNIT	PAPER NUMBER	
WASHING	ron, DC 20	006		2822	
				DATE MAILED: 01/13/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

		i.
4	Application No.	Applicant(s)
SUPPLEMENTAL	08/897,953	KIRA ET AL.
Office Action Summary	Examiner	Art Unit
	David E. Graybill	2822
The MAILING DATE of this communication Period for Reply	on appears on the cover sheet w	ith the correspondence address
A SHORTENED STATUTORY PERIOD FOR F WHICHEVER IS LONGER, FROM THE MAILII - Extensions of time may be available under the provisions of 37 of after SIX (6) MONTHS from the mailing date of this communicat - If NO period for reply is specified above, the maximum statutory - Failure to reply within the set or extended period for reply will, by	NG DATE OF THIS COMMUNION (CFR 1.136(a). In no event, however, may a rion. period will apply and will expire SIX (6) MON	CATION. reply be timely filed ITHS from the mailing date of this communication.
Any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).		
Status		
1)⊠ Responsive to communication(s) filed on	10 November 2005.	
· ·	This action is non-final.	
3) Since this application is in condition for a closed in accordance with the practice up		
Disposition of Claims		
4)⊠ Claim(s) <u>3,5,6,8-10 and 15-17</u> is/are pen 4a) Of the above claim(s) <u>9 and 10</u> is/are 5)☐ Claim(s) is/are allowed. 6)⊠ Claim(s) <u>3,5,6,8 and 15-17</u> is/are rejected 7)☐ Claim(s) is/are objected to. 8)☐ Claim(s) are subject to restriction	withdrawn from consideration.	
Application Papers		
9)☐ The specification is objected to by the Ex	aminer.	
10) The drawing(s) filed on is/are: a)		by the Examiner.
Applicant may not request that any objection	to the drawing(s) be held in abeyar	nce. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the	correction is required if the drawing	(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by t	he Examiner. Note the attached	d Office Action or form PTO-152.
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for for a) All b) Some * c) None of: 1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International E * See the attached detailed Office action for	liments have been received. Iments have been received in A e priority documents have been Bureau (PCT Rule 17.2(a)).	pplication No received in this National Stage
Attachment(s)	F	
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-943) Information Disclosure Statement(s) (PTO-1449 or PTO/92) Paper No(s)/Mail Date 	(s) Paper No(s	Summary (PTO-413) s)/Mail Date. <u>11-10-5</u> . nformal Patent Application (PTO-152)

U.S. Patent and Trademark Office PTOL-326 (Rev. 7-05)

A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 8-31-5 has been entered.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point

out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3, 5, 6, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda (English translation, JP58-180091), and Koga (JP4302444).

In the instant specification, at page 1, line 23 to page 2, line 22, applicant teaches as conventional a process comprising the steps of forming leveled projection electrode studs 14 on a semiconductor chip 11 by wire-bonding; forming conductive adhesive 16a on the electrodes by a conductive adhesive 16 that has been skidded on a plate 15a and then transcribed onto the electrodes; applying a thermosetting insulating adhesive 18 to areas of mounting parts where the chip is to be mounted on a substrate 17; aligning the chip to the mounting parts at a first stage and performing a first fixing of the chips with a first pressure by a bonding head to which the chip is absorbed, the semiconductor chip being pressed separately; and thereafter, heating the substrate on which the chip is fixed with a thermosetting temperature of the adhesive.

However, applicant does not appear to explicitly teach as conventional a process comprising a plurality of chips, and the steps of heating the

adhesive on the substrate with a half-thermosetting temperature so as to harden the adhesive on the substrate to a half-thermosetting state by heating means; moving the substrate to a second stage, while the chips on the substrate are held at their position by the half-thermosetting state of the adhesive; and thereafter, heating at the second stage the substrate on which the chips are fixed.

Nonetheless, Maeda teaches this process at page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full paragraph. Moreover, it would have been obvious to combine the process of Maeda with the process of applicant's admitted prior art because it would enable accurate alignment of plural chips before the final fixing step of the conventional art. Moreover, as can be reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to repeat the process of the semiconductor chip being pressed separately, such that each chip of the plurality of chips of the combination of Maeda and applicant's admitted prior art being pressed separately, to accomplish an expected additive function or result because applicant has not disclosed that, in view of the applied prior art, the limitation that the semiconductor chips each being pressed separately is for a particular unobvious purpose,

produces an unexpected result, or is otherwise critical. Furthermore, it is well established that mere repetition or duplication to accomplish an expected additive function or result is prima facie obvious absent a disclosure that the repetition or duplication is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. See, for example, In re Ockert, 114 USPQ 330 (CCPA 1957); In re Schuelke, 96 USPQ 421 (CCPA 1953); In re Hertrich, 73 USPQ 442 (CCPA 1947); Long Mfg. N.C., Inc. v. Condec Corp., 223 USPQ 1213 (DC ENC 1984); St. Regis Paper Company v. Bemis Company, Inc., 193 USPQ 8 (CA 7 1977); In re Harza 124 USPQ 378 (CCPA 1960); Hofschneider Corp. v. Lane et al., doing business as Lane and Co., 71 USPQ 126 (DC WNY 1946).

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Further, the combination of applicant's admitted prior art and Maeda does not appear to explicitly teach wherein a second fixing is simultaneously performed for each of the chips with a second pressure, the plurality of semiconductor chips being pressed together in the second fixing, and wherein in the heating step (e) while heating the adhesive on the mounting parts a pressure is applied to the chips.

Nevertheless, in the English abstract and figures, Koga teaches a process comprising wherein a second fixing is simultaneously performed for each of plural chips with a second pressure, the plurality of semiconductor chips being pressed together in the second fixing, and wherein in a heating

step while heating an adhesive on mounting parts a pressure is applied to the chips. Furthermore, it would have been obvious to combine the process of Koga with the process of the applied prior art because it would facilitate bonding.

Also, the combination of applied prior art does not appear to explicitly teach a process wherein the second pressure is greater than the first pressure.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure because, as cited, the combination of the applied prior art teaches that a first and second pressure are result effective variables, and applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another relative pressure. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Claims 3, 5, 6, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga as applied

to claims 3, 5, 6, 8 and 15 supra, and further in combination with Sakata (JP4-62946).

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Applicant's admitted prior art, Maeda and Koga do not appear to explicitly teach a process wherein the second pressure is greater than the first pressure.

Notwithstanding, in the English abstract, partial translation, and figures, Sakata teaches this process. Furthermore, it would have been obvious to combine the process of Sakata with the applied prior art because it would enhance production yield.

To further clarify, Sakata teaches that the first pressure is 20 kg/cm² and the second pressure is about 20 kg/cm², and the range encompassed by the phrase "about 20 kg/cm²" encompasses a pressure greater than the first pressure of 20 kg/cm².

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga, as applied to claims 3, 5, 6, 8 and 15, and further in combination with DiStefano (5548091).

Applicant's admitted prior art, Maeda and Koga do not appear to explicitly teach a process comprising wherein, in the heating step (c), heating the adhesive is performed by a heat plate on which the substrate is placed.

Nonetheless, at column 9, lines 3-63, DiStefano teaches a process comprising wherein in a heating step, heating an adhesive is performed by a heat plate 58 on which a substrate mounting chips is placed. In addition, it would have been obvious to combine the process of DiStefano with the process of the applied prior art because, both processes are directed to the same purpose of heating an adhesive, and it would facilitate adhesive curing.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda, Koga and Sakata, as applied to claims 3, 5, 6, 8 and 15, and further in combination with DiStefano (5548091).

DiStefano is applied for the same reasons it is applied supra.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga as applied to claims 3, 5, 6, 8 and 15, and further in combination with Fujimoto (5115545).

Applicant's admitted prior art, Maeda and Koga do not appear to explicitly teach a process comprising a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.

Notwithstanding, as cited, Koga teaches a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is

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provided on the heat block corresponding to the mounting parts of the substrate. Further, at column 6, line 52 to column 7, line 3, Fujimoto teaches a single bonding head 52 for each chip. Moreover, it would have been obvious to combine the process of Fujimoto and the process of Koga by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. Furthermore, it would have been obvious to combine the heat block of Fujimoto and Koga with the applied prior art because it would facilitate bonding.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda, Koga and Sakata as applied to claims 3, 5, 6, 8 and 15, and further in combination with Fujimoto (5115545).

Fujimoto is applied for the same reasons it is applied supra.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (571) 273-8300.

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David E. Graybill Primary Examiner

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D.G. 10-Nov-05